The Design of N bit Quantization Sigma-Delta Analog to Digital Converter

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Abstract-**The paper introduces the principle of sigma-delta ADC modulator with high accuracy and the applied over sampling technique, noise shaping technique and multi-bit quantizer technique. and it makes the behavior level verification for this scheme by Simulink tool in MATLAB. The simulation result Shows that multi-bit quantizer modulator can get very high SNR.**

Keywords: *Sigma-delta ADC; modulator; over sampling; noise shaping; multi-bit quantization.*

1. INTRODUCTION

A sigma−delta modulator is one method for providing the front end to an analog to digital converter. When an analog signal is digitized, quantization error is introduced into the frequency spectrum. The sigma−delta's function is to push the quantization error that is near the signal into a higher frequency band near the sampling frequency. After this is done the signal can be low pass filtered and the original signal can be restored in a digitized for. Over sampling sigma-delta modulation method is one superior way to get the high accuracy converter, this method adopts the over sampling technique and the noise shaping technique of sigma-delta modulator, so it will perform dual suppression for quantization noise in signal frequency band.so it will perform dual suppression for quantization noise in signal frequency band. Finally the down sampling will be performed by the digital decimation filtering. Comparing with other converters with the different structure, sigma-delta ADC has many advantages, such as high accuracy, high linearity and large dynamic range and so on.

2. THEORY OF DELTA-SIGMA MODULATOR FOR ADC

2.1 PRINCIPLE OF DELTA-SIGMA MODULATOR FOR ADC

Figure 1 shows a simple block diagram of a first order sigma delta Analog-to-Digital Converter (ADC). The input signal X comes into the modulator via a summing junction. It then passes through the integrator which feeds a comparator that acts as a one-bit quantizer. The comparator output is fed back to the input summing junction via a one-bit digital-to analog converter (DAC), and it also passes through the digital filter and emerges at the output of the converter. The feedback loop forces the average of the signal W to be equal to the input signal X. A quick review of quantization noise theory and signal sampling theory will be useful before diving deeper into the sigma delta converter.
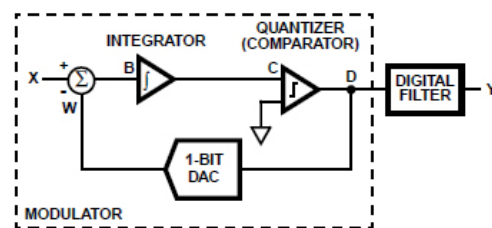

Figure 1. First order sigma delta ADC block diagram

2.2 THE KEY TECHNIQUE OF SIGMA-DELTA MODULATOR

The differences between sigma-delta ADC and general Nyquist converter are that the former adopts the over-sampling and noise shaping technique. Based on these two techniques, the paper designs a high performance sigma-delta ADC modulator. The key techniques are as followed.

2.2.1 OVER-SAMPLING TECHNIQUE

Many applications require measurements using an analog-to-digital converter (ADC).Such applications will have resolution requirements based in the signal's dynamic range ,the smallest change in a parameter that must be measured, and the signal-to-noise ratio (SNR). For this reason, many systems employ a higher resolution off-chip ADC. However, there are techniques that can be used to achieve higher resolution measurements and SNR. This application note describes utilizing oversampling and averaging to increase the resolution and SNR of analog-to-digital conversions. Oversampling ($k*fs>2fm$) and averaging can increase the resolution of a measurement without resorting to the cost and complexity of using expensive. The oversampling is sampling the analog signal whose frequency is much higher than Nyquist sampling frequency. To avoiding the aliasing phenomenon, so the over sampling frequency must be much higher Nyquist sampling frequency. The over sampling frequency (usually between 8 to 512) is defined as the ratio of sampling frequency and Nyquist frequency.
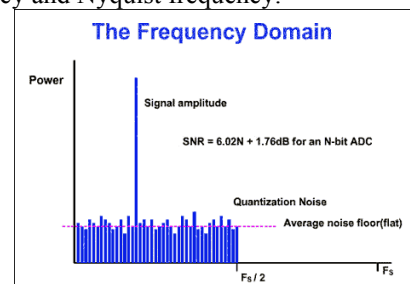

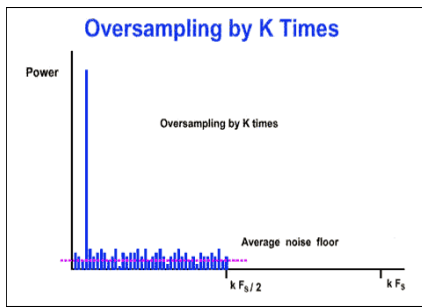Figure 2. Power spectrum of Nyquist sampling frequency

Figure 3. Power spectrum of over sampling frequency

2.2.2 NOISE SHAPING TECHNIQUE

Treating the quantization error can reduce the quantization noise in signal frequency band. The noise shaping technique improves the converting accuracy when analog converting to data. It is assumed that the oversampling input signal has N-bit quantizater, if the oversampling ratio is enough large, then the change of signal is very small in two neighbored sampling process. The quantization noise is alike in the low frequency, the change always appears in the high frequency. So the quantization noise can be decreased in the low frequency band by the method that two successive sampling values subtract. Formula (1) is the principle of one order noise shaping.

$$E(n)=e(n)-e(n-1) \qquad (1)$$

The quantizater noise in frequency band can be further reduced by more number of times sampling values subtract to achieve the high order noise shaping.

2.2.3. MULTI-BIT QUANTIZER TECHNIQUE

To improve the single sigma-delta modulator performance largely, the multiple bits quantizer technique is needed. Sigma-delta modulator with multi-bit quantization structure can increase the convert rate and the resolution of ADC, and it consists of an N-bit parallel ADC and an N-bit DAC. Compared with the single bit quantization modulator, the multi-bit one has many advantages when the conditions are same: it has a bigger stable region, a larger input dynamic range, a higher resolution, in addition, it has a higher linearity. Quantizer is the only nonlinear component in Sigma-delta modulator, but multi-bit quantizer has the good stability and the high linearity, so its performance is close to the linear system . Figure 4 shows the system chart of multi-bit quantization sigma-delta modulator, the output signal Y returns to input port by N-bit DAC.

In sigma-delta modulator circuit, the structure of single bit quantizer is simple. It just needs one comparator and the DAC in the feedback circuit with the stable linearity. However, single bit quantizer has the large quantization noise, and needs the higher OSR to suppress it. Using the single bit quantizer in high order single circuit modulator will make the system become instable. As for the multi-bit quantization, it has higher conversion accuracy, reduces the quantization noise, eliminates the relativity between modulation process and input signal effectively, and enhances the stability of system. While, multi-bit quantization needs adding a multi-bit DAC to the feedback

circuit to produce the feedback signal, which will lead into the nonlinear problem and affect the system's performance, so the calibration is necessary.
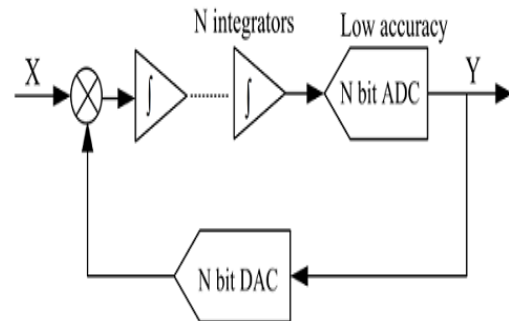

Figure 4: Multi bit quantizer

3 DESIGN OF MULTI-BIT QUANTIZATION SIGMA-DELTA MODULATOR

Sigma-delta modulator is the core part of sigma-delta ADC, and it is composed of the difference summation unit, integrator, quantizer and a DAC. The paper designs a sigma-delta modulator with 24 significant digits, uses Simulink toolbox fully in MATLAB to model the multi-bit quantization sigma-delta modulator, gets its topological structure, and finally designs each module circuit of modulator by using simple components.

3.1. SIGMA-DELTA MODULATOR MODELING

To improve design efficiency and reduce design period, it must adopt one fast and flexible circuit simulation scheme with high accuracy to design the high accuracy Sigma-delta modulator. Meanwhile, it must make the circuit structure adjustment and parameters optimization to get the high resolution and large dynamic range. The design adopts single circuit three orders CIFF circuit, and the ideal model of multi-bit quantization sigma-delta modulator is established by Simulink in MATLAB. It is shown in Figure 5.
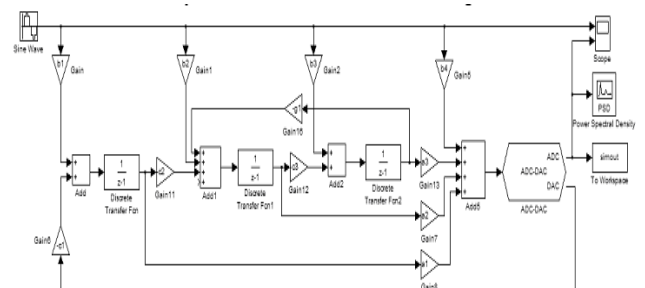

Figure 5: Multi-bit quantization Sigma-delta Modulator's Ideal Model

3.2. SIGMA-DELTA MODULATOR CIRCUIT DESIGN

Sigma-delta modulator includes integrator, quantizer and DAC. The paper designs a low cost and high performance sigma-delta modulator through simple discrete device. It adopts 3-bit quantizer and feedback DAC. Compared with others, they can be achieved easily and their cost is low. The each part circuit is as followed.

3.2.1. INTEGRATOR DESIGN

The integrator is the core circuit module of sigma-delta modulator. Here we adopt the switched capacitor

integrator, which consists of the switch, sampling integrating capacitor and operational amplifier. Figure 6 describes the three stages integrator with switched capacitor. A voltage follower between input port and first stage integrator is designed to lead into the negative feedback with voltage series. The input impedance of voltage follower is high, while the output impedance is low, so it can achieve the impedance match and isolation between former and latter stages.
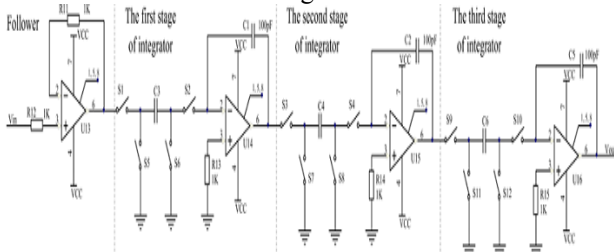

Figure 6: Three Orders Paralleled Integrator

3.2.2 DAC DESIGN:

The output of quantizer gets to the first integrator through the feedback of DAC. The feedback loop can make the input port of the first integrator tend to zero, namely, the input value of modulator is equal to the average value of DAC's output. In this paper, we use 3-bit feedback ADC, which is composed of multiple switch 74HC4053, operational amplifier, and exclusions. Due to the low cost and fast speed of multiple switch, and similar performance in exclusion, they are appropriate to used as feedback ADC whose accuracy is very high. Its structure is shown in Figure 7.
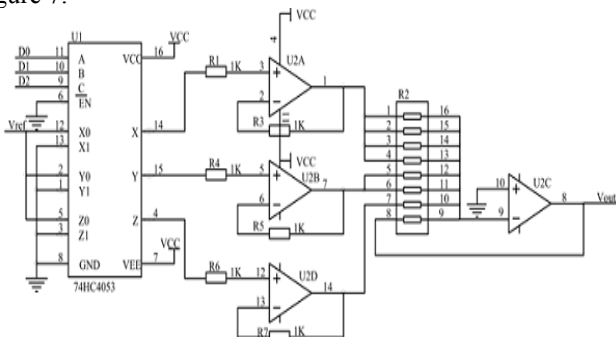

Figure 7: Feed back ADC

3.2.3 QUANTIZER DESIGN

The quantizer is a 3-bit successive approximation ADC, and is composed of a comparator, D/A converters, buffer registers and control logic circuits. The structure of D/A converter is shown in Figure 6, and the control logic of it is realized in FPGA. The basic principle is that, comparing levels from high bit to low bit, as if using balance to weigh objects, we should increase or decrease weights step by step from heavy to light. The process of successive approximation conversion is as follows: clear every bit in the register when initializing, and the supreme bit will be set "1" and be sent into D/A convert at the beginning of conversion. The output of D/A convert is analog, i.e., Vo. Then compare it with Vi, which is also an analog signal waiting to be converted. If Vo<Vi, the 1 in this bit is kept, otherwise it will be cleared. Then the second high bit will

be set "1" and be sent into D/A convert, Vo compares with Vi, If Vo<Vi, the 1 in this bit is kept, otherwise it will be cleared. Repeat this process until the lowest bit of the successive approximation register. After the transformation, send every digital quantity into the buffer register, and get the digital output. All these processes are controlled by a circuit. Because the 3-bit successive approximation ADC can be achieved by sample discrete components, and doesn't need photolithographic process, thus it has low cost and high convert rate.

4. SIMULATION EXPERIMENT RESULT

The paper simulates the 3-bit quantization sigma-delta modulator under the conditions that the over-sampling rate is 256. Here we use the Simulink toolbox in MATLAB. Figure 8 shows the input wave and output wave of modulator, the red line presents the input wave, and the blue line is output wave. Figure 9 shows the performance of multi-bit quantization modulator model while Figure 10 shows the performance of modulator model with 1-bit quantization.
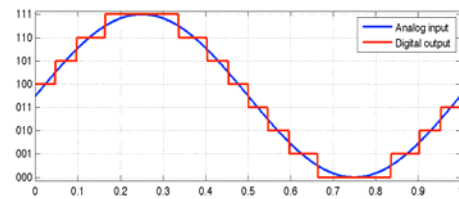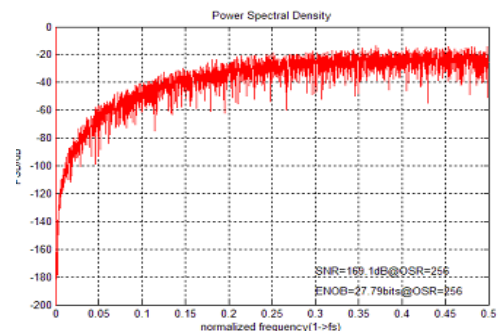

Figure 8: Input and output Waveforms

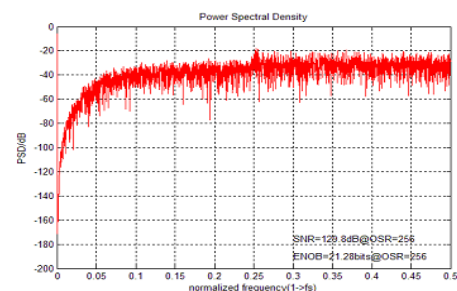Figure 9: multi bit quantization modular model

Figure 10: single bit quantization modular model

The simulation results show that, the wave groove in Figure 8 is wider than it in Figure 9, and the SNR is evidently higher than it by one bit quantization. When sampling rate is 256, the resolution of 3-order 3-bit quantization sigma delta modulator is 27.79 bits when the SNR is 169.1dB, while the resolution of 1-bit quantization sigma-delta modulator is 21.28 bits when SNR is 129.8 dB

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